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U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10043276	01/14/2002	438	14	2812	

**APPLICANTS: Nakatani Goro; Sakamoto Tatsuya;

**CONTINUING DATA VERIFIED: JmL
none

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** FOREIGN APPLICATIONS VERIFIED: JmL
JAPAN 2001-6581 01/15/2001

DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no	ATTORNEY DOCKET NO
35 USC 119 conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no	040894-5755
Verified and Acknowledged Examiners's initials JmL	
TITLE : Semiconductor device and method for manufacturing the same	

U.S. DEPT. OF COMM./PAT. & TM-PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
Amount Due	Date Paid		Total Claims	Print Claim for O.G.
ISSUE FEE		Primary Examiner	DRAWING	
Amount Due	Date Paid		Sheets Drwg.	Figs. Drwg.
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE	Application Examiner	
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